Amendments to the Claims

Please cancel claims 1 - 36 and add new claims 37- 43 as follows:

1-36 (Cancelled)

37. (New) A memory for access by a circuit simulation program comprising:

an encapsulated circuit model stored in the memory, the circuit model being behaviorally equivalent to an original circuit, the circuit model comprising:

at least one output node and one input node;

a first current source having a first current value and being connected to a voltage source and the output node;

and second current source having a second current value and being connected to the output node and ground;

a first input voltage value;

a first output voltage value;

a first capacitor connected to the input node and ground and having a first capacitance value;

a second capacitor connected to the input node and the output node and having a second capacitance value; and

a third capacitor connected to the output node and ground and having a third capacitance value;

wherein the circuit simulation program configures a computer system to calculate an output node value on the output node of the encapsulated circuit model;

the output node value is a function of the first and second current value, the first input voltage value, the first output voltage value, and the first, second and third capacitance

value;

wherein the first and second current value, and the first, second, and third capacitance value, is calculated by the computer system as a function of the first input voltage value and the first output voltage value.

the computer system further stores in the memory, the input voltage value, the output voltage value, the first and second current value, the first, second, and third capacitance value, and the output node value;

the circuit simulation program accesses the memory to retrieve the output node value; and

the encapsulated circuit model stored in the memory exhibits none of a plurality of circuit details from the original circuit.

38. (New) The encapsulated circuit model of claim 37, wherein the circuit simulation program configures the computer system to calculate, and store in the memory, a plurality of the first and a plurality of second current values, a plurality of the first capacitance values, a plurality of the second capacitance values, and a plurality of the third capacitance values, for each of a plurality of the input voltage values and a plurality of the output voltage values over a user-defined input and output voltage range.

39. (New) The encapsulated circuit model of claim 38, wherein the circuit simulation program configures the computer system to calculate a plurality of the output node values for each of the plurality of the input voltage values and for each of the plurality of the output voltage values over the user-defined input and output voltage range;

each of the plurality of the output node values being a function of each of the corresponding plurality of: the first and second current values, and the first, second, and third capacitance values.

40. (New) The circuit model of claim 37, wherein an output load is connected to the output node and has an output load value; the output load comprises:
a fourth capacitor connected to the output node and ground;
a resistor connected to the output node and a second output node; and
a fifth capacitor connected to the second output node.

41. (New) The circuit model of claim 37, wherein the first current source is a p-block behavioral model which stored in the memory; and
the second current source is an n-block behavioral model which is stored in the memory.

42. (New) The circuit model of claim 38, wherein the circuit model further comprises a plurality of the input nodes each having an input voltage value and a plurality of the output nodes, each having an output voltage value, wherein each of the plurality of the input nodes corresponds to one each of the plurality of the output nodes;

for each of the input nodes and the output nodes is a plurality of the first current sources; wherein each of the plurality of the first current sources is connected to a portion of the plurality of the input nodes and a portion of the plurality of the output nodes;

for each of the input nodes and the output nodes is a plurality of the second current sources; wherein each of the plurality of second current sources is connected to a portion of the plurality of the input nodes and a portion of the plurality of the output nodes; and

wherein each of the plurality of the input nodes and each of the corresponding plurality of the output nodes is coupled to one each of a plurality of the second capacitors.

43. (New) The circuit model of claim 37 further comprising

an impedance value measured from the output node and ground;

wherein the output node value is a function of the first and second current value, the first input voltage value, the first output voltage value, the first, second and third capacitance value and the impedance value;

wherein the first current value, the second current value the first, second, and third capacitance value, and the impedance value, is calculated by the computer system as a function of the first input voltage value and the first output voltage value;

the computer system further stores in the memory, the input voltage value, the output voltage value, the first and second current value, the first, second, and third capacitance value, the impedance value, and the output node value.

44. (New) The circuit model of claim 43, wherein the impedance value is derived from a pi model connected between the output node and ground.

45. (New) A memory for access by a circuit simulation program comprising:

an encapsulated circuit model stored in the memory, the circuit model being behaviorally equivalent to an original circuit, the circuit model comprising:

at least one output node and one input node;

a first input voltage value;

a first output voltage value;

a first current source having a first current value and being connected to a voltage source and the output node;

a first capacitor connected to the input node and ground and having a first capacitance value;

a second capacitor connected to the input node and the output node and having a second capacitance value; and
a third capacitor connected to the output node and ground and having a third capacitance value;

wherein the circuit simulation program configures a computer system to calculate an output node value on the output node of the encapsulated circuit model;

the output node value is a function of the first current value, the first input voltage value, the first output voltage value, and the first, second and third capacitance value;

wherein the first current value, and the first, second, and third capacitance value, is calculated by the computer system as a function of the first input voltage value and the first output voltage value.

the computer system further stores in the memory, the input voltage value, the output voltage value, the first current value, and the first, second, and third capacitance value, and the output node value;

the circuit simulation program accesses the memory to retrieve the output node value; and

the encapsulated circuit model stored in the memory exhibits none of a plurality of circuit details from the original circuit.

46. (New) The encapsulated circuit model of claim 45, wherein the circuit simulation program configures the computer system to calculate, and store in the memory, a plurality of the first current values, a plurality of the first capacitance values, a plurality of second capacitance values, and a plurality of the third capacitance values, for each of a plurality

of the input voltage values and a plurality of the output voltage values over a user-defined input and output voltage range.

47. (New) The encapsulated circuit model of claim 46, wherein the circuit simulation program configures the computer system to calculate a plurality of the output node values for each of the plurality of the input voltage values and for each of the plurality of the output voltage values over the user-defined input and output voltage range;

each of the plurality of the output node values being a function of each of the corresponding plurality of: the first current values, and the first, second, and third capacitance values.

48. (New) The circuit model of claim 45, wherein an output load is connected to the output node and has an output load value; the output load comprises a fourth capacitor connected to the output node and ground;
a resistor connected to the output node and a second output node; and
a fifth capacitor connected to the second output node.

49. (New) The circuit model of claim 45, wherein the circuit model further comprises a plurality of the input nodes each having an input voltage value and a plurality of the output nodes, each having an output voltage value each having an output voltage value, wherein each of the plurality of the input nodes corresponds to one each of the plurality of the output nodes;

for each of the input nodes and the output nodes is a plurality of the first current sources; wherein each of the plurality of the first current sources is connected to a portion of the plurality of the input nodes and a portion of the plurality of the output nodes.

wherein each of the plurality of the input nodes and each of the corresponding plurality of the output nodes is coupled to one each of a plurality of the second capacitors.

50. (New) The circuit model of claim 45 further comprising

an impedance value measured between the output node and ground;

wherein the output node value is a function of the first current value, the first input voltage value, the first output voltage value, the first, second and third capacitance value and the impedance value;

wherein the first current value, the first, second, and third capacitance value, and the impedance value, is calculated by the computer system as a function of the first input voltage value and the first output voltage value;

the computer system further stores in the memory, the input voltage value, the output voltage value, the first current value, the first, second, and third capacitance value, the impedance value, and the output node value.

51. (New) The circuit model of claim 50, wherein the impedance value is derived from a pi model connected between the output node and ground.